

REMARKS

Claims 1, 7-12, and 22 remain pending in this application.

The Examiner rejected claims 1, 7-12, and 22 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,428,673 (*Ritzdorf*). Applicants respectfully traverse this rejection.

In the Final Office Action dated November 24, 2003, the Examiner stated that Applicant's argument regarding multiple measurements for each data point is based upon a first and a second false premise. Applicants respectfully beg to differ. Applicants respectfully assert that "multiple measurement for each data point" in *Breiner* does not refer to plurality of measurements at different points on a semiconductor wafer. The evidence and reasoning for support this assertion is provided below. When examining this phrase, one skilled in the art would not ignore the disclosure in *Breiner* that actually sheds light to this phrase. As disclosed in *Breiner*, the "number of points" reference in *Breiner* refers to the number of positions in the fabrication process, not the number of points on the semiconductor wafer itself (the evidence for supporting this statement is on col. 4, lines 14-15). Additionally, the term "wafer map" is specifically separated to discuss electrical testing and refers to electrical test characteristics, such as breakdown voltages, leakage currents, resistivity, *etc.* *Breiner* discloses using such data to provide a wafer map relating to electrical responses related to the geography of the semiconductor wafer (see item numbers 8 and 9 on col. 4, lines 48-59). Nothing in *Breiner*, or in the other cited prior art, suggests a wafer map relating to the thickness across various portions of the semiconductor wafer.

Although **Breiner** discloses wafer thickness, **Breiner** actually points to using wafer maps for electrical testing. **Breiner** intentionally omits the discussion of wafer maps when discussing other types of data, such as deposition data, etch data, photolithography data, CMP data, and implant data (see items listed on col. 4, lines 18-59). In a parallel list that discusses various types of data, **Breiner** intentionally leaves out the term “wafer map” when discussing all items, except for discussion of electrical test. Therefore, **Breiner** actually suggests to only using wafer maps for electrical type data. Therefore, **Breiner** actually teaches away from the claimed invention.

Additionally, **Breiner** only provides a passing reference to a “mean” value of data points, as described above, **Breiner** does not disclose measuring the thickness of copper layers at a plurality of locations on the copper layer and averaging the resultant data, as called for by the claims of the present invention. Again, the term “mean value” is put into context by the preceding term “multiple measurements for each data point,” which suggest a mean or median value for the multiple measurements for each data point and not to same measurements of different data points (see col. 4, lines 61-65). Furthermore, claims 1 and 22 (as amended) also call for measuring a mechanical stress and modifying a parameter relating to forming a copper layer, which is not disclosed or made obvious by the cited prior art. Support for these amendments may be found in the specification, for example, see page 12 of the specification. Therefore, **Breiner** clearly does not disclose or make obvious all of the elements of the claimed invention. Furthermore, as discussed below, the addition of subject matter disclosed by from **Ritzdorf** and **Wolf** to the disclosure of **Breiner** would still not disclose or make obvious all of the elements of the claimed invention.

As explained in the previous Response to Office Action and as provided below, Applicants do not address the cited art separately. Instead Applicants provide evidence of no anticipation and non-obviousness of the claims by providing various cites in the prior art and accompanying arguments. Applicants clearly demonstrate herein that the cited prior art, individually and in combination do not disclose or make obvious all of the elements of the claimed invention.

Independent claims 1 and 22 are allowable for at least the reasons cited above. Additionally, dependent claims 7-12, which depend from independent claim 1, are also allowable for at least the reasons cited above.

The Examiner rejected claims 1, 7, 8, 10, 11, and 22 under 35 U.S.C. § 103(a) as being unpatentable over *Ritzdorf* in view of Silicon Processing for the VLSI Era, Vol. 1-Process Technology, 2nd ed., Lattice Press: Sunset Beach, CA 2000, pp. 799-800 (*Wolf*), and U.S. Patent No. 6,211,094 (*Jun*). Applicants respectfully traverse this rejection.

Ritzdorf (even when considered with *Wolf* and *Jun*) does not teach, disclose, or suggest all of the elements of claims 1, 7-12 and 22. *Ritzdorf* is directed towards a system for receiving a wafer for processing, *e.g.*, electrochemical plating. *Ritzdorf* discloses forming a seed layer upon a wafer, and transporting the wafer for further analysis or processing (see, for example col. 9, lines 52-55, col. 10, lines 14-16). However, *Ritzdorf* does not disclose forming an opening upon a first dielectric layer that is formed above a first structure, upon which a copper layer is formed and controlling a parameter based upon a measured thickness, as called for by claims 1 and 22 (as amended) of the present invention.

Additionally, *Ritzdorf*, or any other art cited in the Office Action, does not disclose averaging the thickness data from a plurality of sites on a copper layer, as called for by claims 1 and 22 (both as amended). Controlling a parameter in response to thickness data that is averaged from data relating to a plurality of positions are among the concepts that are not disclosed by *Ritzdorf*, but are called for by claims 1 and 22 of the present invention. Additionally, adding the disclosure of the damascene process in *Wolf*, along with the disclosure of *Jun*, still would not anticipate all of the elements of claim 1, 7-12 and 22. *Wolf* describes depositing metal and dielectric layers (see 2nd paragraph, page 800 of *Wolf*), but fails to disclose averaging the thickness data from a plurality of sites on a copper layer or modifying a parameter in response to the averaged thickness data, as called for by claims 1 and 22 (both as modified). *Jun* merely discloses measurement wafers that are analyzed for thickness at various zones. However, *Jun* does not disclose various elements that are missing from the combination of *Wolf* and *Ritzdorf*, such as the assessment of the mechanical stress in combination with the thickness analysis. Therefore, adding the disclosure of *Wolf* and *Jun* to the disclosure of *Ritzdorf* would not result in all of the elements called for by claims 1 or 22 (both as amended) of the present invention.

Furthermore, based upon at least the arguments provided above, Applicants respectfully disagree with the Examiner that some of the elements called for by claim 1 may be inherent in light of *Wolf*, *Jun*, and *Ritzdorf*, as the Examiner does not provide evidence to support such an argument. In light of the arguments provided above, all of the elements of claim 1 (as amended) of the present invention are not disclosed, taught, or suggested by *Ritzdorf*, *Wolf*, *Jun*, or their combination. Thus, claim 1 is allowable. Additionally, for at least the reasons presented above, claim 22 (as amended), which has similar “means” elements relating to the elements of claim 1, claim 22 is also allowed.

Independent claims 1 and 22 are allowable for at least the reasons cited above. Additionally, dependent claims 7, 8, 10, and 11, which depend from independent claim 1, are also allowable for at least the reasons cited above.

In light of the arguments presented above, Applicants respectfully assert that claims 1, 7-12 and 22 are allowable. In light of the arguments presented above, a Notice of Allowance is respectfully solicited.


If for any reason the Examiner finds the application other than in condition for allowance, the **Examiner is requested to call the undersigned attorney** at the Houston, Texas telephone number (713) 934-4069 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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